REMARKS

Claims 1-65 are pending in the present application. Claims 54 and 65 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 54-56 and 65 stand rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* (U.S. Patent No. 6,510,503). Claims 1-4, 6-9, 11 and 60-61 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth (U.S. Patent No. 6,029,250). Claim 5 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth, and further in view of Gasbarro, *et al.* (U.S. Patent No. 5,432,823). Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Moyal, *et al.* (U.S. Patent No. 6,326,853). Claim 12 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Wada, *et al.* (U.S. Patent No. 6,029,250). Claims 13-15 and 22-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Yoshitake (U.S. Patent No. 6,043,704). Claim 57 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Chan, *et al.* (U.S. Patent No. 5,998,860). Reconsideration and removal of the rejections and allowance of the claims are respectfully requested.

With regard to the rejection of claims 1 and 60, in the present invention as claimed in independent claim 1, a memory system having a stub configuration includes a controller for generating a first clock signal. A memory module receives the first clock signal from the controller and, in response to a write command, initiates a write operation for writing data signals from a data bus to memory devices in synchronization with the first clock signal, and in response to a read command, initiates a read operation for reading data from the memory device to the data bus in synchronization with the first clock signal, and generates a second clock signal in response to the first clock signal, and the data signals and the second clock signal are output from the

memory module in synchronization with the first clock signal. In this manner, the "first clock signal" that the data signals written from the data bus to the memory devices are in synchronization with during a write operation is the same "first clock signal" that the data read from the memory devices to the memory bus are in synchronization with during a read operation, and the same "first clock signal" that the second clock signal is generated in response to, and the same "first clock signal" that the data signals and the second clock signal are output from the memory module in synchronization with during the read operation.

In the present invention as claimed in independent claim 60, a method of transferring data in a memory system having a stub configuration includes generating a first clock signal at a controller. The method further includes in response to a write command, a memory module initiating a write operation for writing data signals from a data bus to memory devices in synchronization with the first clock signal, and, in response to a read command, the memory module initiating a read operation for reading data from the memory devices to the data bus in synchronization with the first clock signal, generating a second clock signal in response to the first clock signal and outputting the data signals and the second clock signal in synchronization with the first clock signal. In this manner, the "first clock signal" that the data signals written from the data bus to the memory devices are in synchronization with during a write operation is the same "first clock signal" that the data read from the memory devices to the memory bus are in synchronization with during a read operation, and the same "first clock signal" that the second clock signal is generated in response to, and the same "first clock signal" that the data signals and the second clock signal are output from the memory module in synchronization with during the read operation.

Gillingham, *et al.* is cited in the Office Action as disclosing a memory system having a stub configuration (see Gillingham, *et al.* column 10, lines 10-57 and column 11, lines 23-59). A controller 82 generates a free running reference clock CLK. Source synchronous data clocks dclk0 and dclk1 are provided by the controller 82 for timing data in a source synchronous manner. During a read operation, memory devices 84 drive one of the data clocks dclk0 and

dclk1 in a source synchronous manner along with read data on the data bus, and the controller 82 schedules which of the data clocks to use, such that the controller 82 knows which data clock to use to latch in read data.

It is stated in the Office Action with regard to independent claims 1 and 60 that Gillingham, *et al.* does not discuss the details of clock generations in the memory module. Thus, Gillingham, *et al.* fails to teach or suggest a memory system that includes a "memory module" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 1. In addition, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system that includes, in response to a "write command", a memory module "initiating a write operation for writing" "data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and, in response to a "read command", the memory module "initiating a read operation", "generating a second clock signal in response to the first clock signal" and "outputting the data signals and the second clock signal in synchronization with the first clock signal", as claimed in claim 60.

Keeth discloses a read clock signal RCLK that is apparently derived from a clock generator 40 that generates a number of clock signals to be used on the memory module 404, in response to a received command clock CCLK (see FIG. 3 of Keeth and the corresponding discussion at column 3, lines 48-53). A read synchronization system 400 of Keeth includes a read FIFO buffer 420 that generates differential data clock signals DCLK0 and DCLK1 in response to the read clock signal RCLK (see Keeth, FIG. 4). Data packet words D<0:15> are captured by the memory controller 402 responsive to the data clock signals DCLK0 and DCLK1.

Keeth fails to teach or suggest a memory system that includes a "memory module" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 1. Keeth in no way teaches that the D<0:15> signals and the DCLK0 and DCLK1 signals returned from the memory module 404 during a read operation are in synchronization with a clock signal that is also in synchronization with data signals being written from the Keeth data bus DQ to the Keeth memory devices of the Keeth memory module 404 during a write operation. Further, Keeth fails to teach or suggest a method of transferring data in a memory system that includes, in response to a "write command", a memory module "initiating a write operation for writing" "data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and, in response to a "read command", the memory module "initiating a read operation", "generating a second clock signal in response to the first clock signal" and "outputting the data signals and the second clock signal in synchronization with the first clock signal", as claimed in claim 60 for similar reasons.

Neither Gillingham, *et al.* nor Keeth teaches or suggests a memory system that includes a "memory module" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 1. Further, neither Gillingham, *et al.* nor Keeth teaches or suggests that a method of transferring data in a memory system includes, in response to a "write command", a memory module "initiating a write operation for writing" "data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and, in response to a "read command", the memory module "initiating a read operation", "generating a

second clock signal in response to the first clock signal" and "outputting the data signals and the second clock signal in synchronization with the first clock signal", as claimed in claim 60. Accordingly, it is submitted that the combination of Gillingham, *et al.* nor Keeth fails to teach or suggest the invention as claimed in claims 1 and 60. Reconsideration of the rejection of, and allowance of, claims 1 and 60 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* and Keeth are respectfully requested. With regard to the dependent claims 3-4, 6-9, 11 and 61, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejection of claim 5 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Gasbarro, *et al.*, Gasbarro, *et al.* is cited in the Office Action as disclosing a system wherein the propagation delay of a clock signal from a device to a master is substantially equal to that of a data bus. Like Gillingham, *et al.* and Keeth, Gasbarro, *et al.* fails to teach or suggest a memory system that includes a "memory module" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 1. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Gasbarro, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 5 are respectfully requested.

With regard to the rejection of claim 10 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Moyal, *et al.*, Moyal, *et al.* is cited in the Office Action as disclosing a system comprising a capacitor having a capacitance that is selected to compensate for capacitive loading. Like Gillingham, *et al.* and Keeth, Moyal, *et al.* fails to teach or suggest a memory system that includes a "memory module" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data

signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 1. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Moyal, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 10 are respectfully requested.

With regard to the rejection of claim 12 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Wada, *et al.*, Wada, *et al.* is cited in the Office Action as disclosing a memory system wherein first and second signal lines are crossed between first and second modules. Like Gillingham, *et al.* and Keeth, Wada, *et al.* fails to teach or suggest a memory system that includes a "memory module" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 1. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Wada, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 12 are respectfully requested.

With regard to the rejection of claims 13-15 and 22-24 under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.*, Keeth, and Yoshitake, Yoshitake is cited in the Office Action as disclosing a system wherein a return clock signal line is coupled to a dummy load. Like Gillingham, *et al.* and Keeth, Yoshitake fails to teach or suggest a memory system that includes a "memory module" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a

"read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 1. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Yoshitake fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claims 13-15 and 22-24 are respectfully requested.

With regard to the rejection of independent claims 54 and 65, in the present invention as claimed in independent claim 54, a memory system having a stub configuration includes a controller for generating a first clock signal, a memory module including memory devices coupled to the controller, and a second clock signal generator independent of both the controller and the memory module for generating a second clock signal. The memory module receives the first clock signal and the second clock signal.

In the present invention as claimed in independent claim 65, a method of transferring data in a memory system having a stub configuration includes generating a first clock signal at a controller, and generating a second clock at a second clock signal generator independent of both the controller and a memory module including memory devices coupled to the controller. The method further includes receiving the first clock signal and the second clock signal at the memory module.

Gillingham, *et al.* fails to teach or suggest a memory system that includes "a controller for generating a first clock signal", "a memory module including memory devices coupled to the controller", and a "second clock signal generator independent of both the controller and the memory module for generating a second clock signal", as claimed in claim 54. Instead, in Gillingham, *et al.*, during a read operation, memory devices 84 drive one of the data clocks dclk0 and dclk1 in a source synchronous manner along with read data on the databus and the controller 82 schedules which of the data clocks should be used, such that the controller knows which data clock to use to latch in read data. Therefore, Gillingham, *et al.* does not disclose a "second clock

signal generator independent of both" a "controller" and a "memory module" as claimed in claim 54. Further, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system that includes "generating a second clock at a second clock signal generator independent" of "both" a "controller" and a "memory module", as claimed in claim 65. Instead, in Gillingham, *et al.*, during a read operation, memory devices 84 drive one of the data clocks dclk0 and dclk1 in a source synchronous manner along with read data on the databus and the controller 82 schedules which of the data clocks should be used, such that the controller knows which data clock to use to latch in read data. Reconsideration and removal of the rejection of claims 54 and 65 under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* are therefore respectfully requested. With regard to the dependent claims 55 and 56, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejection of independent claim 57, under 35 U.S.C. 103(a) as being unpatentable over the combination of Gillingham, *et al.*, Keeth and Chan, *et al.*, in the present invention as claimed in independent claim 57, a memory system having a stub configuration includes a controller for generating a first clock signal. A memory module having first and second faces, in response to a write command, initiates a write operation for writing data signals from a data bus to memory devices in synchronization with the first clock signal, and in response to a read command, initiates a read operation for reading data from the memory device to the data bus in synchronization with the first clock signal, and generates a second clock signal in response to the first clock signal, and the data signals and the second clock signal are output from the memory module in synchronization with the first clock signal.

As stated above, Gillingham, *et al.* fails to teach or suggest a memory system that includes a "memory module having first and second faces" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the

"memory module in synchronization with the first clock signal", as claimed in claim 57.

Also, as stated above, Keeth fails to teach or suggest a memory system that includes a "memory module having first and second faces" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 57.

Chan, *et al.* discloses a double-sided inline memory module 20 (see Chan, *et al.*, FIG. 1). Like Gillingham, *et al.* and Keeth, Chan, *et al.* fails to teach or suggest a memory system that includes a "memory module having first and second faces" that receives a "first clock signal" from a "controller" and, in response to a "write command", initiates "a write operation for writing data signals from" a "data bus" to "memory devices in synchronization with the first clock signal", and in response to a "read command", generates a "second clock signal in response to the first clock signal", and the "data signals and the second clock signal" are output from the "memory module in synchronization with the first clock signal", as claimed in claim 57. Accordingly, it is submitted that the combination of Gillingham, *et al.*, Keeth and Chan, *et al.* fails to teach or suggest the invention as claimed. Reconsideration of the rejection of, and allowance of, claim 57 are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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